

IN THE CLAIMS:

The status and content of each claim follows.

1. (previously presented) A circuit in an embedded processing system covering a number of technical applications, a number of operative functions of the number of technical applications being performed via a respective number of application-specific Electronic Control Units (ECU), the circuit comprising:

a) a number of controller means for controlling respective application specific ECUs, each of the controller means comprising a number of application-specific support functions and I/O subsystems; and

b) a number of processor units each having an I/O-interface operatively connecting to a respective one of the controller means and supplying that controller means with computing power,

wherein at least one of the processor units and a respective controller means are implemented on different chips.

2. (previously presented) The circuit according to claim 1, further comprising mapping means for mapping the I/O subsystems to the processor units, and a General Controller Unit operatively coupled to the mapping means and configured to dynamically switch at least one of the processor units into communication with a selected controller means based on processor timing requirements.

3. (previously presented) The circuit according to claim 2, further comprising:
a primary layer comprising basic configuration layout data and an interface means for connecting to the number of processor units; and
a secondary layer comprising a preprogrammed, autonomic state switching means, a preprogrammed emergency switching means, and a port interface means connected to at least one of the I/O subsystems.
4. (previously presented) The circuit according to claim 3, further comprising an additional controller operatively coupled to the General Controller Unit and configured to implement a monitoring function for monitoring the operational status of the processor units and the controller means.
5. (previously presented) The circuit according to claim 1, further comprising a database storing instructions on how to handle specific errors associated with the number of processor units.
6. (currently amended) The circuit according to claim 1, further comprising a number of emergency controllers (~~110, 112~~) for continuously storing current global positioning system (GPS) coordinates and configured to send an emergency signal including the coordinates in case a number of external sensor devices detect an emergency case.

7. (previously presented) An embedded system having an electronic circuit according to claim 1.

8. (previously presented) A method of operating an embedded processing system comprising:

controlling a number of electronic control units with a number of interface expander controllers, wherein said interface expander controllers are disposed on a separate chip from said electronic control units; and

providing computing power to said interface expander controllers with a separate number of processors.

9. (previously presented) The method of claim 8, further comprising selectively providing communication between said interface expander controllers and said processors with a General Controller Unit.

10. (previously presented) The method of claim 8, further comprising disposing said interface expander controllers on a single Application Specific Integrated Circuit.